AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions and listings of claims in the application:

LISTING OF THE CLAIMS:

Claims 1-20 (Cancelled)

21. (Original) A semiconductor device comprising: a memory controller receiving commands from a CPU, and controlling a memory including a plurality of memory banks, wherein said memory controller has a first mode and a second mode, wherein each of said plurality of memory banks comprises a plurality of word lines, data lines, and memory cells, wherein said memory is controlled to precharge after a read access in said first mode, wherein said memory is controlled to receive next access command without precharge operation after a read access in said second mode, wherein when a refresh command is received by said memory controller, said memory controller precharges said plurality of memory cells of said plurality of memory banks before refreshing said plurality of memory cells.

22. (Original) The semiconductor device according to claim 21, wherein a successive read acc ss after refresh command is operated without a precharge operation.

23. (Original) The semiconductor device according to claim 22, wherein said memory controller comprises a page access decision circuit, a mode changing circuit, and an address generating circuit, wherein said page decision circuit compares a row address inputted to said memory controller and the previous address, wherein said mode changing circuit receives signals from said page decision circuit and holds information of a number of consecutive access to each of said plurality of said memory banks, and wherein said address generating circuit receives signals from said page decision circuit and from said mode changing circuit and outputs bank active commands, bank addresses, row addresses, and column addresses to said memory.

24. (Original) The semiconductor device according to claim 23, wherein said memory controller further comprises a first and a second bus coupled to said address generating circuit, wherein said first bus is used for transferring commands and said second bus is used for transferring addresses.

25. (Original) The semiconductor device according to claim 23, wherein said memory is a SDRAM.

26. (Original) The semiconductor device according to claim 24, further comprising: a DRAM memory chip to be controlled by said memory controller, wherein said DRAM memory chip is molded in the same package as the memory controller.

27. (Original) The semiconductor device according to claim 24, wherein during said first mode if an access to a same word line continues, a precharge operation before a read operation is abridged, wherein during said second mode if an access to a different word line occurs, a precharge is operated before a read operation.